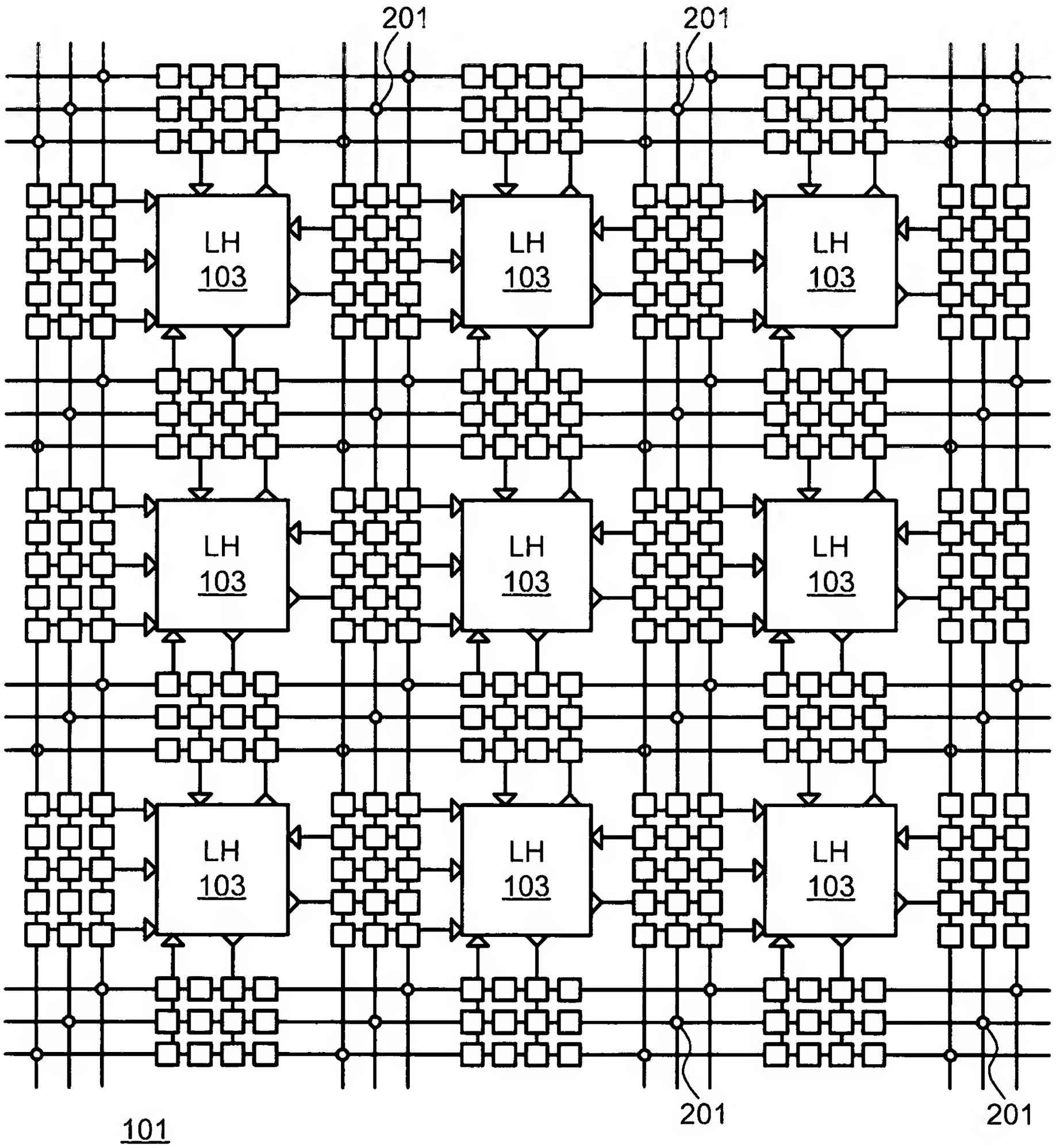


FIGURE 1

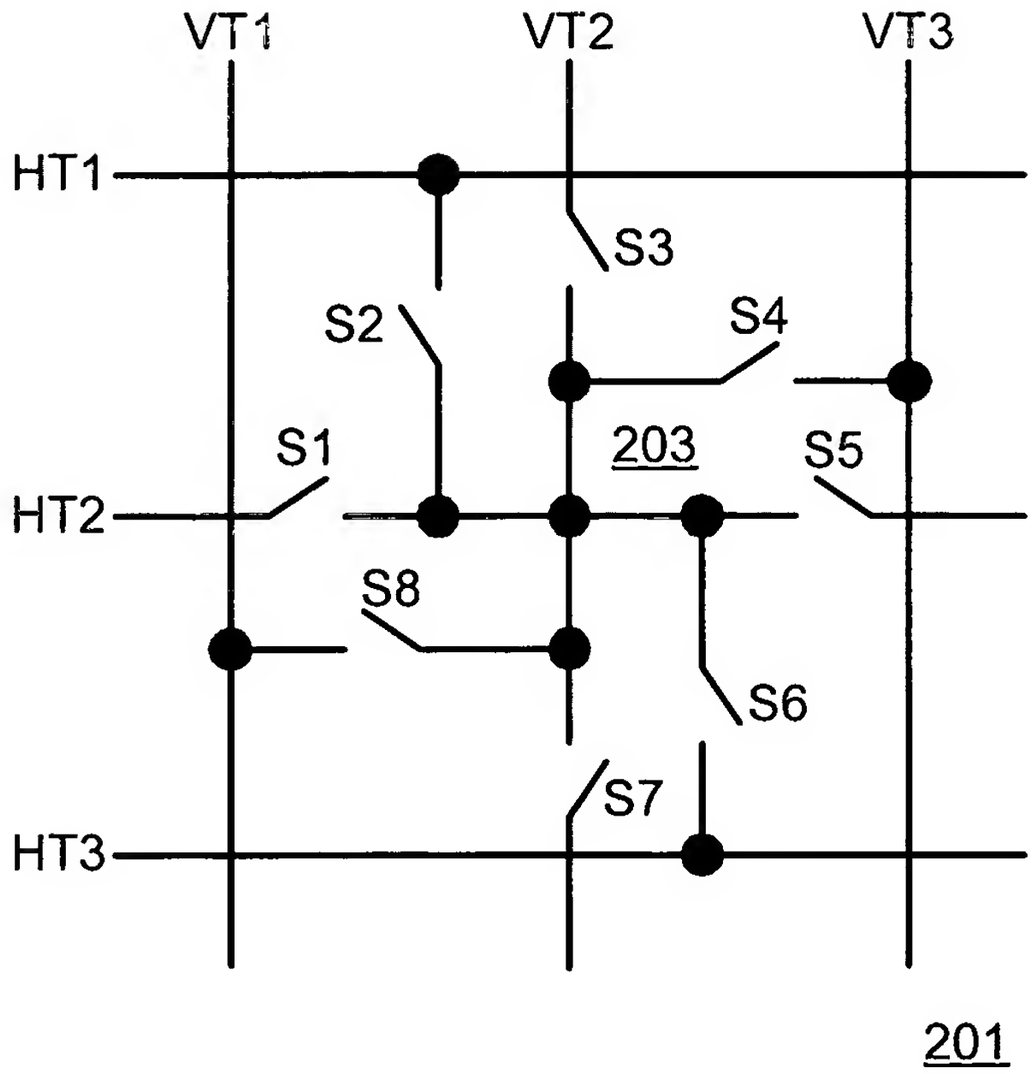
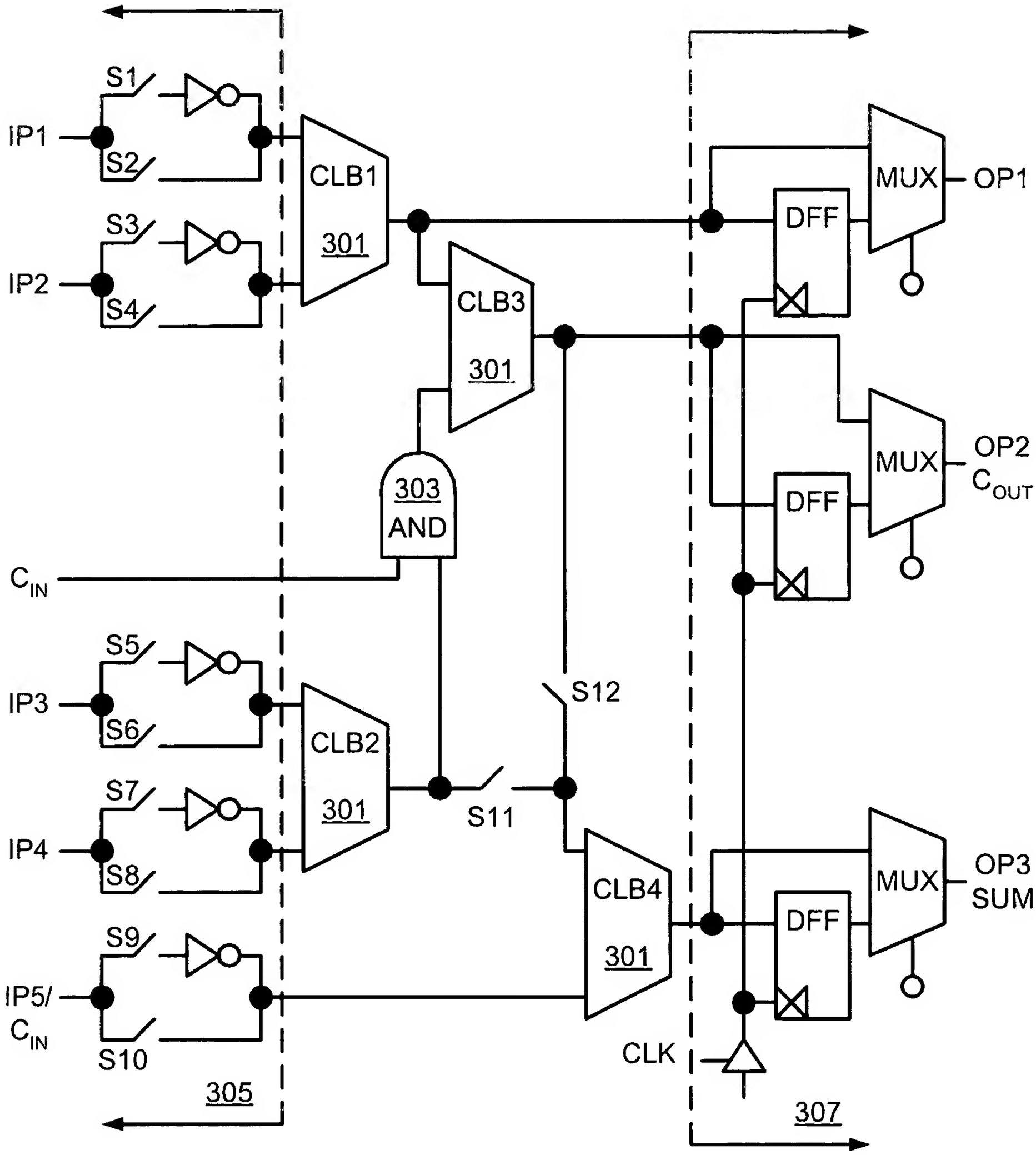


FIGURE 2



CLB : CASCADABLE LOGIC BLOCK

FIGURE 3

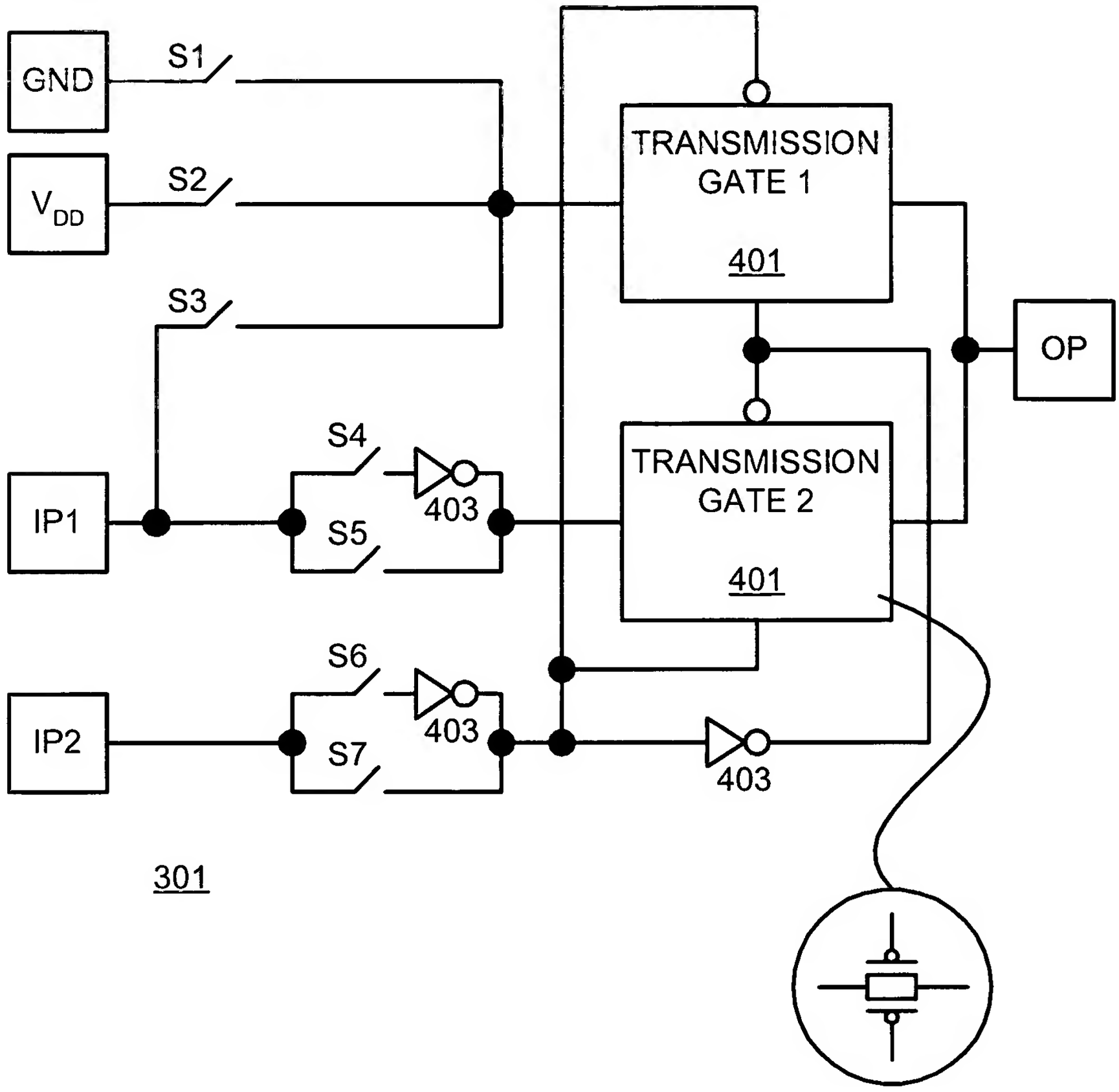

GND
S1
V_{DD}
S2
S3
IP1
S4
S5
403
IP2
S6
S7
403
TRANSMISSION GATE 1
401
TRANSMISSION GATE 2
401
403
OP
301

FIGURE 4

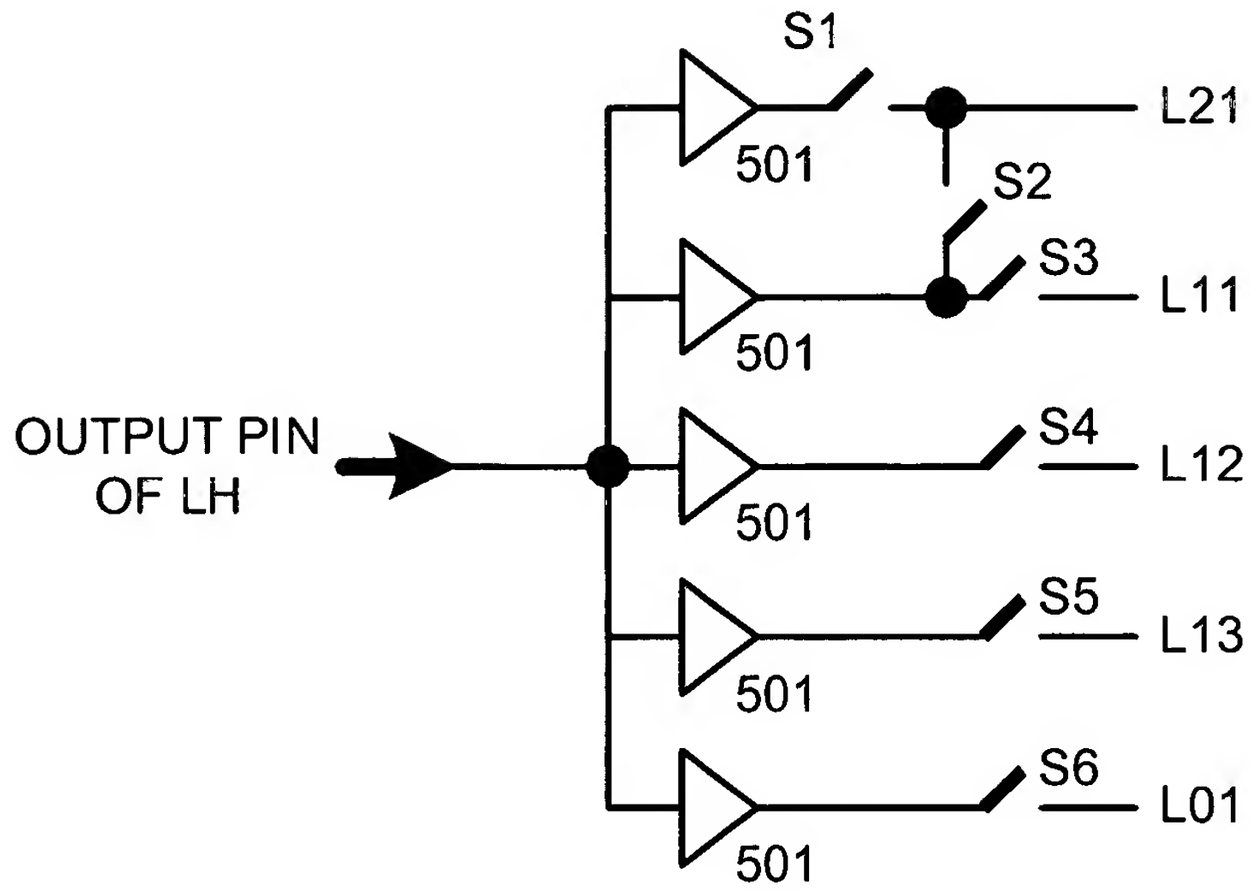
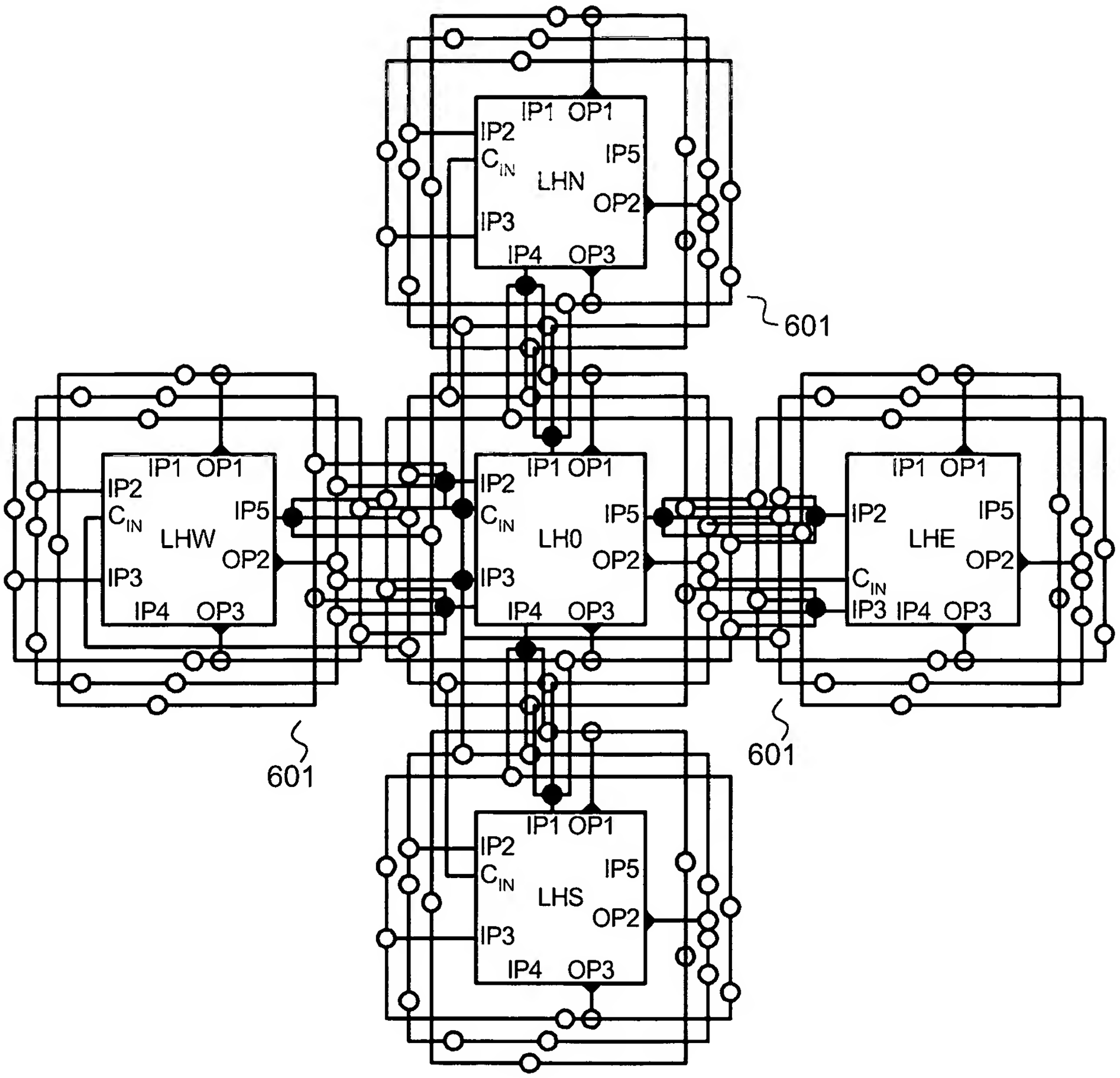

S1
L21
501
S2
S3
L11
501
OUTPUT PIN
OF LH
S4
L12
501
S5
L13
501
S6
L01
501

FIGURE 5



- PASS TRANSISTOR OR SWITCH
- HARD WIRED
- BUFFER

FIGURE 6

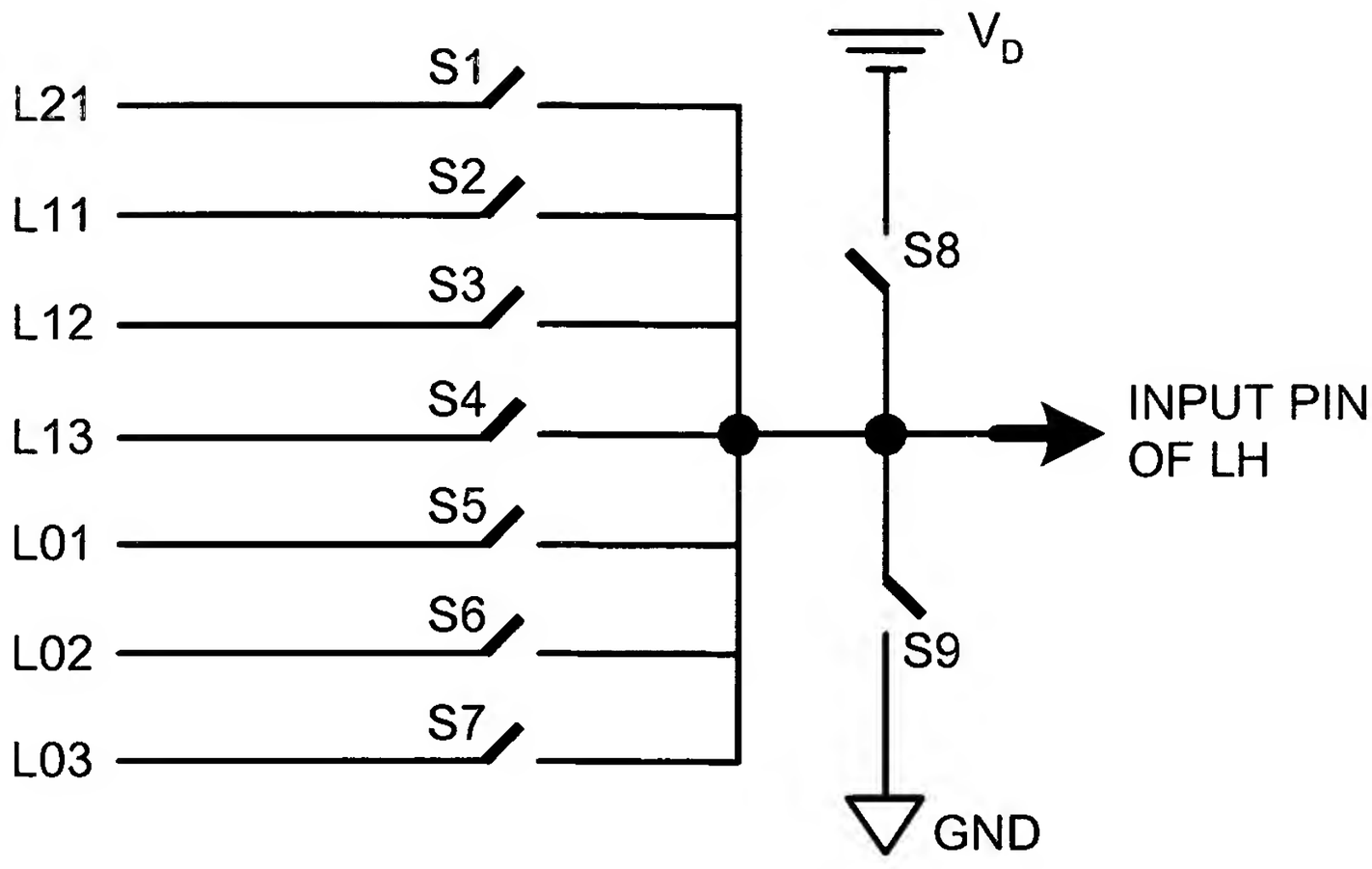

L21
L11
L12
L13
L01
L02
L03
S1
S2
S3
S4
S5
S6
S7
S8
S9
V_D
INPUT PIN
OF LH
GND

FIGURE 7

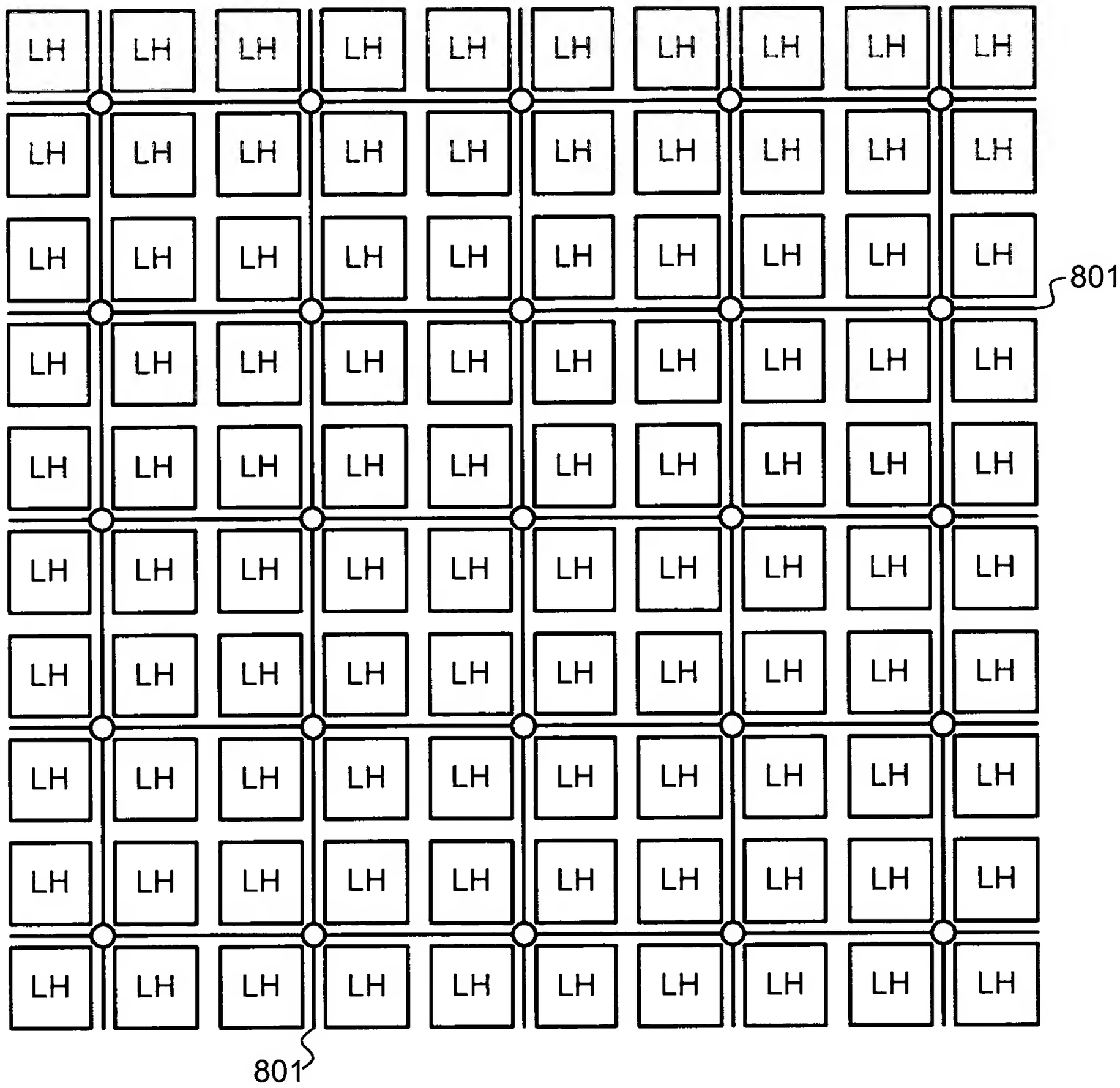


FIGURE 8

SWITCH	S1	S2	S3	S4	S5	S6	S7	EQUATION
AND2	✓	✗	✗	✗	✓	✗	✓	OP = IP1 & IP2
NAND2	✗	✓	✗	✓	✗	✗	✓	OP = !(IP1 & IP2)
OR2	✗	✓	✗	✗	✓	✓	✗	OP = IP1 | IP2
NOR2	✓	✗	✗	✓	✗	✓	✗	OP = !(IP1 | IP2)
XOR2	✗	✗	✓	✓	✗	✗	✓	OP = (IP1 & !IP2) | (!IP1 & IP2)
XNOR2	✗	✗	✓	✓	✗	✓	✗	OP = (IP1 & IP2) | (!IP1 & !IP2)

NOTE: ✓ : SWITCH ON ✗ : SWITCH OFF

FIGURE 9

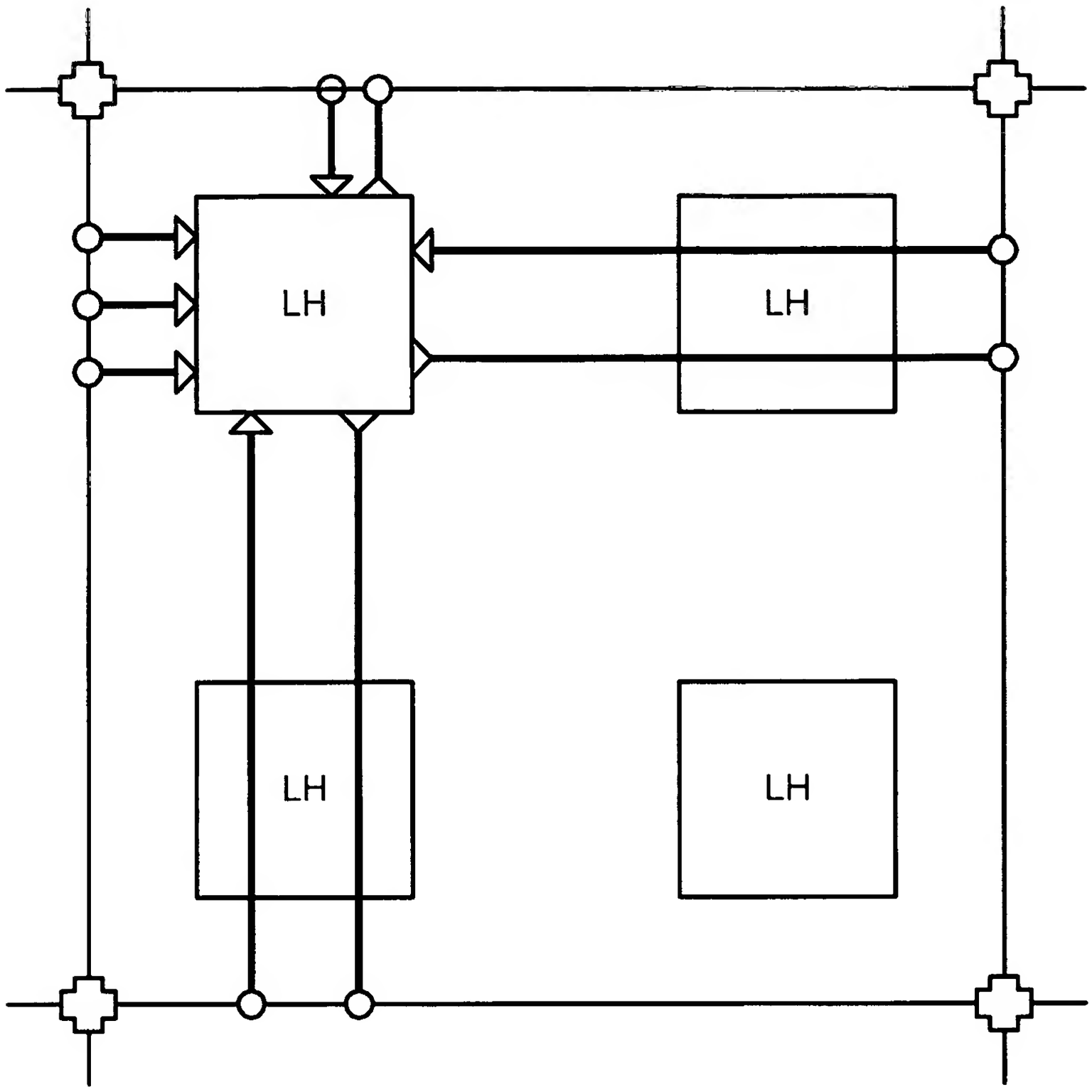


FIGURE 10